

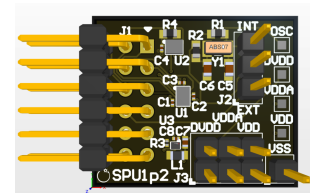
EVB PCB Schematics and Pinouts

The SPU-001 EVB PCB can be used with any host with an SPI interface and 1.8-3.3V logic.

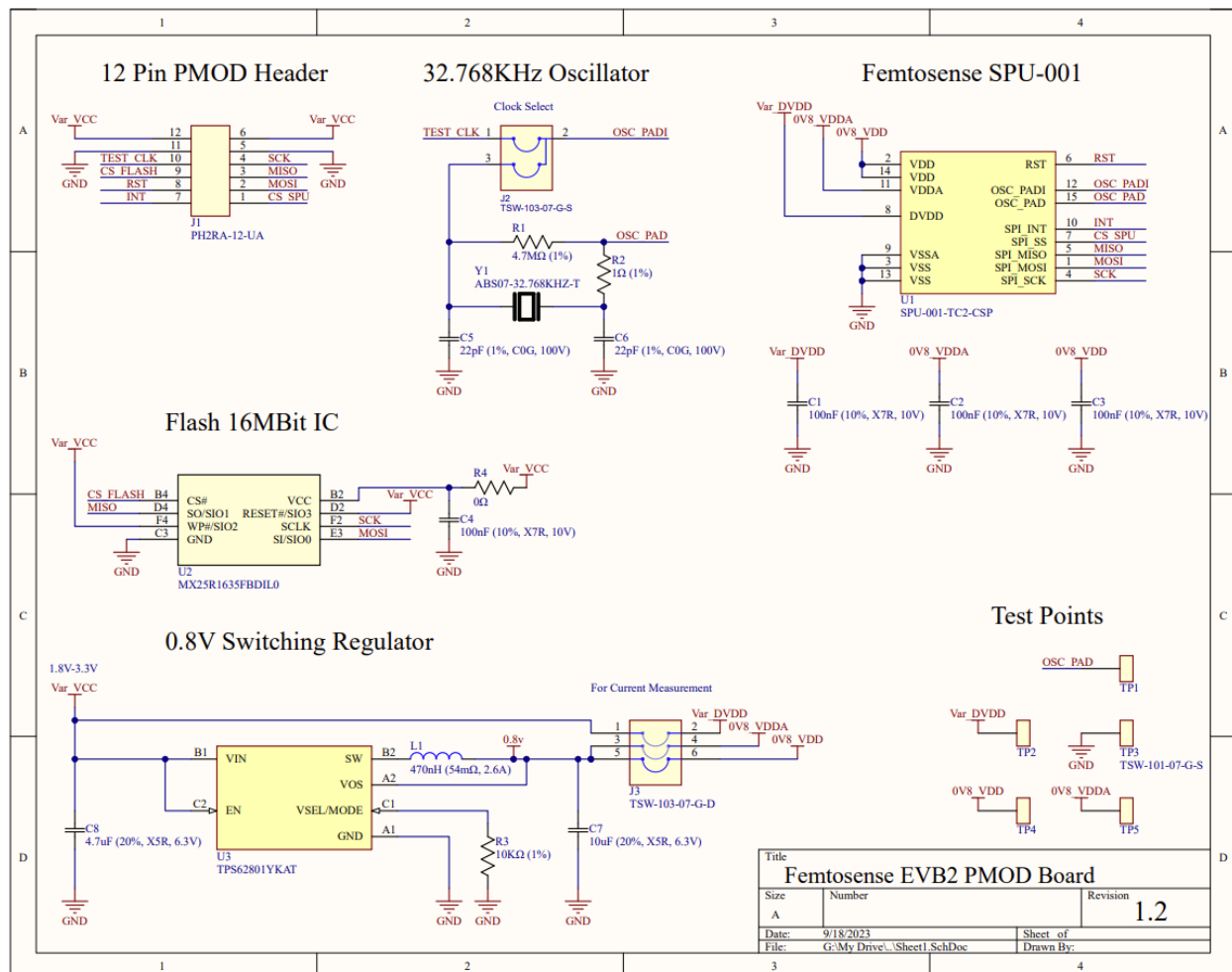
There are two variations available:

- EVB2: SPU-001-CSP package
- EVB3: SPU-001-QFN package

These boards are generally backwards compatible. The schematics are given below:



EVB2

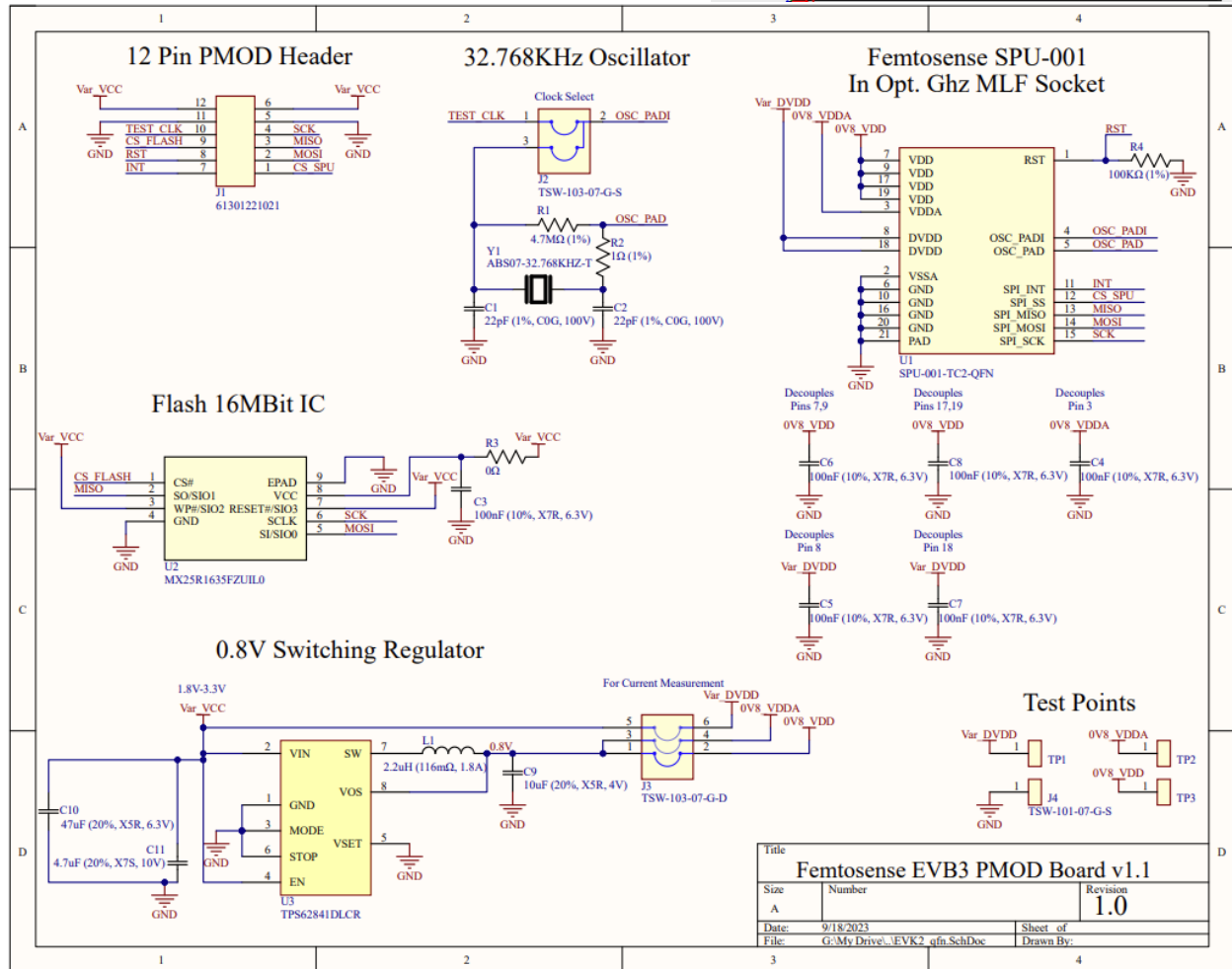
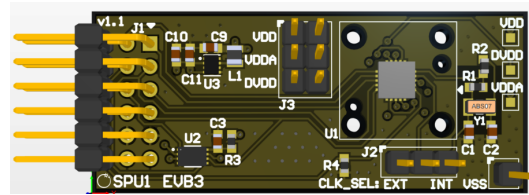


SPU-001 Evaluation Kit

Application Note 002

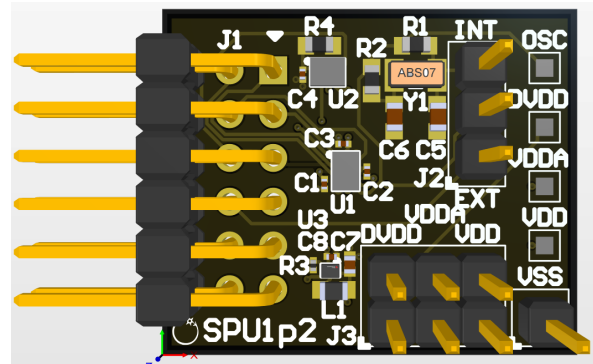
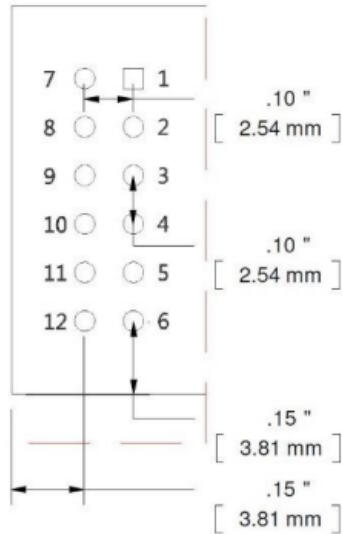
FEMTOSENSE

EV3



Application Note 002

The pinout of the main header J1 is pin-compatible with the Digilent PMOD interface type 2A specification:



EVB2 shown, but EVB3 pinout is the same

Pin	Description	Note
1	SPI Chip Select for SPU-001	active low
2	SPI MOSI signal	
3	SPI MISO signal	
4	SPI SCK clock signal	
5	Ground	
6	VCC	1.8V-3.3V
7	SPU Interrupt signal	logic high when data frame is ready
8	SPU Reset signal	active high
9	SPI Chip Select for onboard flash chip	PN: Macronix MX25R1635FBDIL0
10	Reference Clock for SPU	
11	Ground	
12	VCC	1.8V-3.3V

Note: All IO should be conducted at VCC level.

Application Note 002

Jumpers

The following jumpers should be configured as follows:

Pin	Description	Configuration
DVDD	IO power rail, VCC	connect jumper vertically (EVB2) or horizontally (EVB3)
VDDA	PLL power rail, 0.8v	connect jumper vertically (EVB2) or horizontally (EVB3)
VDD	Main power rail, 0.8v	connect jumper vertically (EVB2) or horizontally (EVB3)
J2 (CLK_SEL)	Reference Clock selector	INT position: onboard oscillator EXT position: reference clock from J1 pin 10

Change Log

Version	Release Date	Description
1.0	2023-05-04	Initial release
1.1	2023-07-23	Updated schematic with typo
1.2	2023-09-18	Added EVB3