FEMTOSENSE

Application Note 005

This Application Note explains latency in the SPU system when running the AINR application and describes how to measure it.

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End-to-end Latency and its Components

The latency of an AI Noise Reduction (AINR) system consists of three parts:

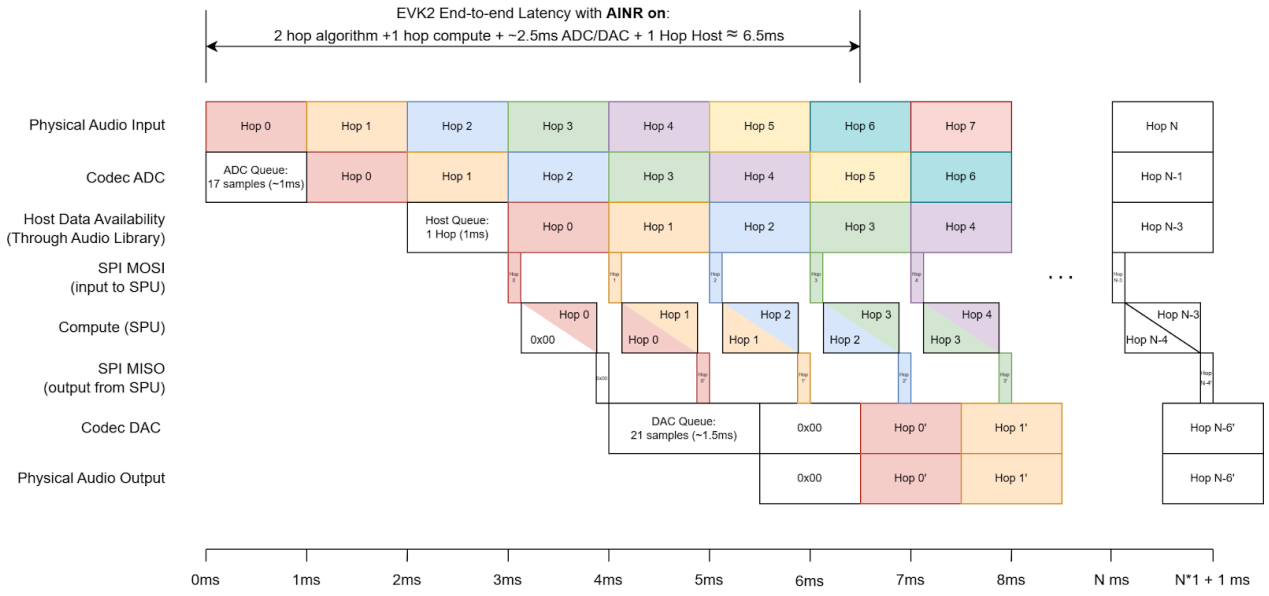
- **Algorithm Latency**: Latency inherent to the algorithm due to the overlap-add associated with the Short-Time Fourier Transform and its inverse. Each audio frame received by the SPU is processed alongside the previous input frame. This step generates an output audio frame corresponding to the previous input frame. The resulting latency is 2x the hop size, where the hop size is the time between audio frames.
- **Compute Latency**: Time taken by the SPU to compute the algorithm. This is at most 1x the hop size, as the algorithm must complete once per audio frame to keep up with the audio stream.
- **Additional System Latency**: Host buffering in the microcontroller, codec, analog-to-digital converter, and digital-to-analog converter, if any. On the Femtosense EVK2, the host consists of a Teensy 4.1 microcontroller and TI TLC320AIC3206 audio codec. After firmware implementation, this latency is:
  17 sample ADC queue + 21 sample DAC queue + 1 hop host audio queue

Summing these parts results in the **End-to-end Latency**.

As an example, when using 16KHz audio and a 1ms hop AINR algorithm on the EVK2, the End-to-end Latency is then:

2ms algorithm + 1ms compute + (~1ms ADC queue + ~1.5ms DAC queue + 1ms host queue) ≈ 6.5ms

The figure below details the latency of the audio samples as they are processed:

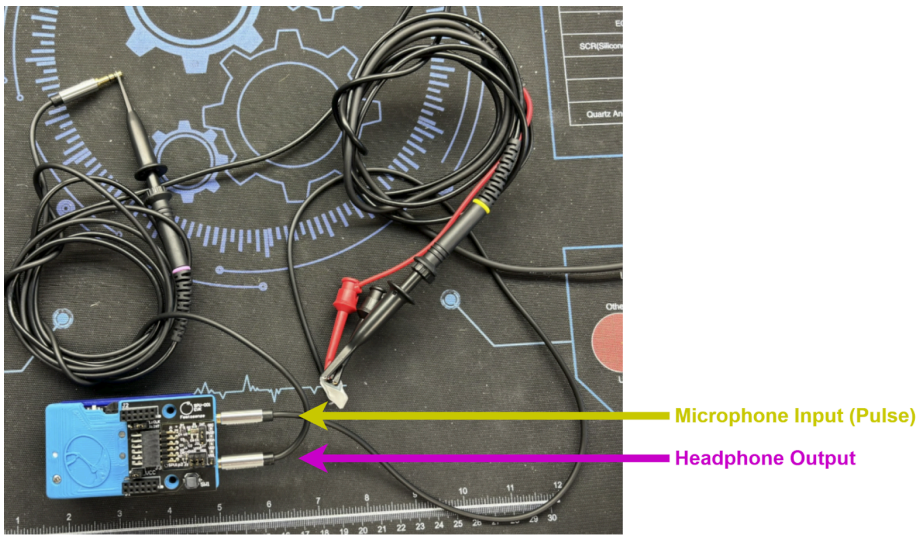


Measuring Latency

Latency can be measured by inputting a pulse into the EVK microphone input, and measuring when the pulse is returned at the headphone output. The pulse can be audible to the internal mic, or fed into the microphone jack using a signal generator. If using the microphone jack, you must include the following line in your 0PROG_P file:

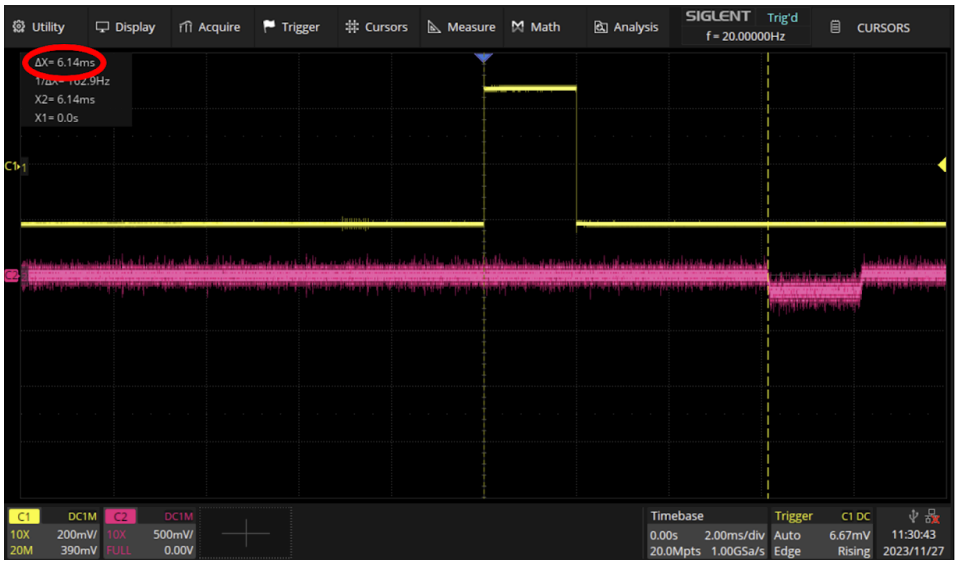
```
USE_EXTERNAL_MIC 1
```

The following photo shows the external microphone setup connected to an oscilloscope and signal generator:



The following figure shows the resulting measurement of the 6.5ms End-to-end latency of AINRGP_16khz_1hop_2algo_v0:

The following figure shows the resulting measurement of 6.14ms End-to-end latency of a different algorithm, AINRGP_16khz_1hop_2algo_v1, which is more optimized for low-latency by reducing the compute time by increasing the SPU clock speed:



End-to-end latency can also be measured on EVK3, where the Additional System Latency introduced by the host and audio codec is less than that of EVK2.

Change Log

Version	Release Date	Description
1.0	2023-12-21	Initial release